



## **STA1600** **10600 x 10600 Element Image Area** **Full Frame CCD Image Sensor**

### **FEATURES**

- 10580 x 10560 Photosite Full Frame CCD Array
- 9  $\mu\text{m}$  x 9  $\mu\text{m}$  Pixel
- 95.22mm x 95.05mm Image Area
- 100% Fill Factor
- Readout Noise Less Than 20 Electrons at 10MHz
- Dynamic Range > 75dB
- 16 Two Stage Source Follower Output Channels
- Three-Phase Buried Channel NMOS Image area
- Three-Phase Buried Channel Readout Registers
- Multi-Pinned Phase (MPP) optional

### **GENERAL DESCRIPTION**

The STA1600 is a 10580 x 10560 image element solid state Charge Coupled Device (CCD) Full Frame sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The STA1600 is organized in two halves each containing an array of 10580 horizontal by 5280 vertical photosites. The pixel spacing is 9 $\mu\text{m}$  x 9 $\mu\text{m}$ . For dark reference, each readout line is preceded by 8 dark pixels. This imager is available in a full frame transfer configuration (shown) or a split frame transfer configuration with shield metalization covering half of the imager. The split frame transfer architecture allows higher frame rate operation through four readout quadrants, whereas the single-sided approach allows readout through two readout quadrants. The STA1600 is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

### **FUNCTIONAL DESCRIPTION**

The following functional elements are illustrated in the block diagram:

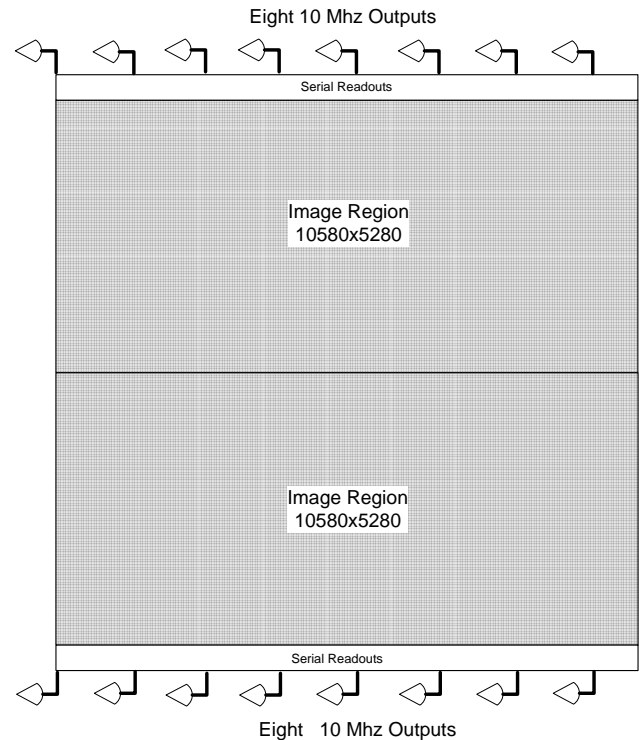
**Image Sensing Elements:** Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.

**Vertical Charge Shifting:** The Full Frame architecture of the STA1600 provides video information as a single sequential readout of 5280 lines containing 1330 photosite. At the end of an integration period the  $\phi_{A_1}$ ,  $\phi_{A_2}$ , and  $\phi_{A_3}$  clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into an Upper and Lower half. Each 10580 x 5280 half may be clocked independently or together. Horizontal Transport registers along the top and bottom permit simultaneous readout of both halves. The STA1600 may be clocked such that the full array is readout by the Upper or Lower Transport registers.

**Horizontal Charge Shifting:**  $\phi_{S_1}$ ,  $\phi_{S_2}$  and  $\phi_{S_3}$  are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for



vertical binning. For both frame transfer configurations, the charge may be read out through the eight amplifiers at the bottom or top of the image frame storage region

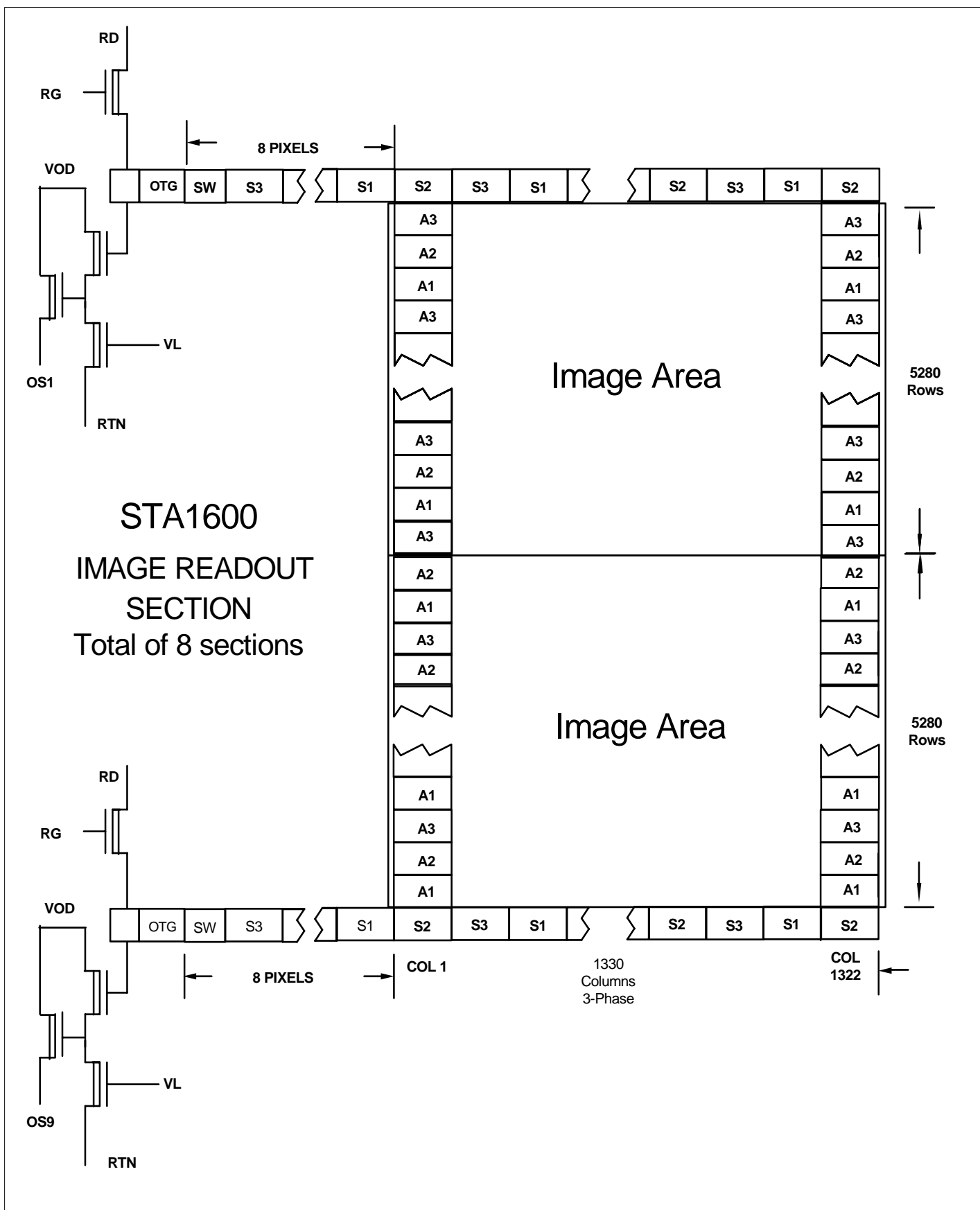
The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 8 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

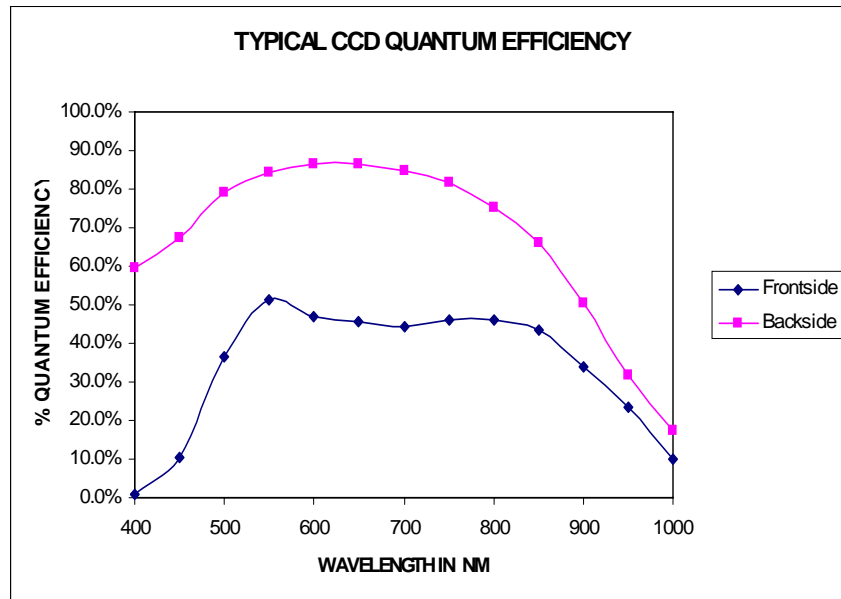
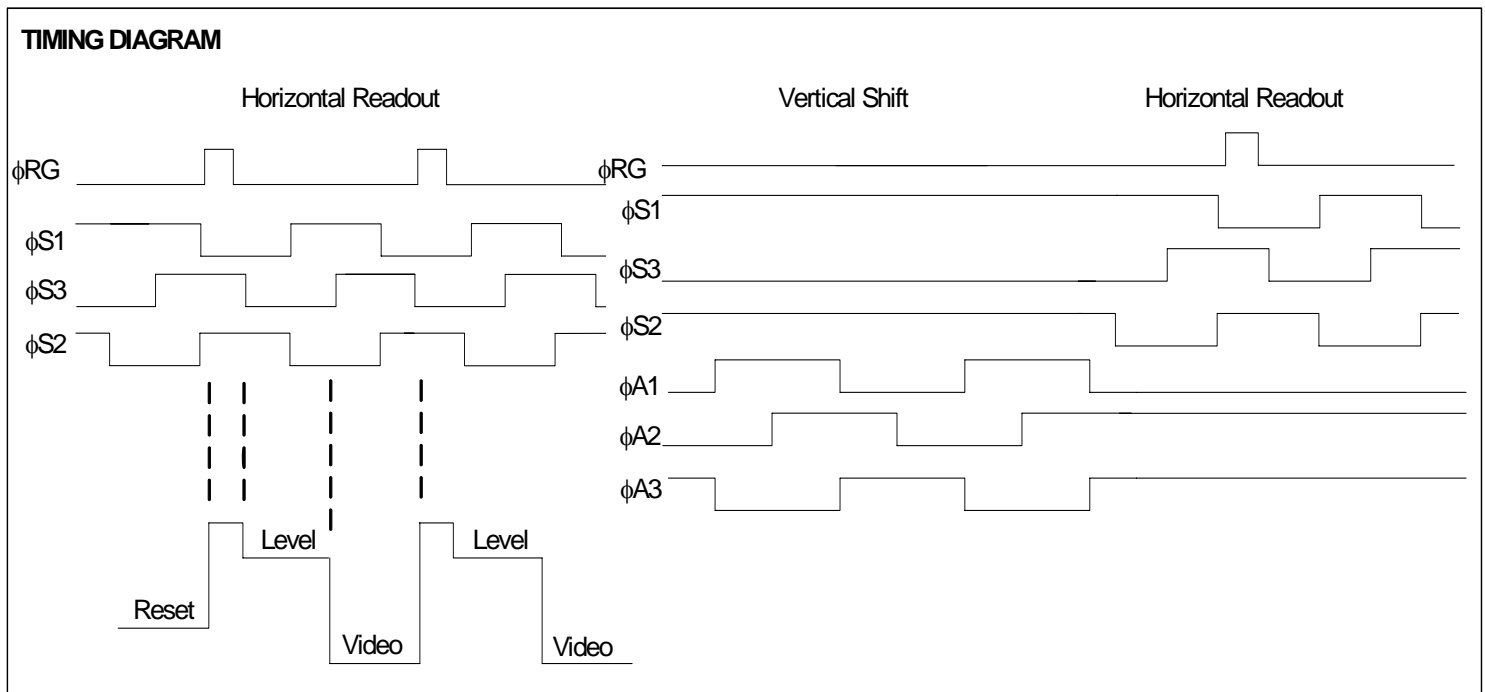
The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to  $\phi_{H_2}$  for normal full resolution readout.

The reset FET in the horizontal readout, clocked appropriately with  $\phi_R$ , allows binning of adjacent pixels.

**Output Amplifier:** The STA1600 has one output amplifier at the end of each Horizontal register. They are dual FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output  $V_{os}$  pin is produced. The capacitor is then reset via the reset MOSFET with  $\phi_{RG}$  to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. The output amplifier drain is tied to VOD. The source is connected to an external load resistor to ground and constitutes the video output from the device.





## DEFINITION OF TERMS

**Charge-Coupled Device** A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

**Vertical Transport Clocks**  $\phi_{A1}$ ,  $\phi_{A2}$ ,  $\phi_{A3}$  the clock signals applied to the vertical transport register.

**Horizontal Transport Clocks**  $\phi_{S1}$ ,  $\phi_{S2}$ ,  $\phi_{S3}$  the clock signals applied to the horizontal transport registers.

**Reset Clock**  $\phi_{RG}$  the clock applied to the reset switch of the output amplifier.

**Dynamic Range** The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

**Saturation Exposure** The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

**Spectral Response Range** The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

**Photo-Response Non-Uniformity** The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

**Dark Signal** The output signal is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

**Vertical Transfer Gate  $\phi$ VTG** Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in

parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

**Pixel** Picture element or sensor element, also called photo element or photosite

### DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V <sub>OD</sub>	DC Supply Voltage		25.0		V	
V <sub>RD</sub>	Reset Drain Voltage		16.0		V	
V <sub>OTG</sub>	Output Voltage	-2.0	1.0	2.0	V	
V <sub>SS</sub>	Substrate Ground		0.0		V	

### TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
V $\phi$ <sub>S(1,2,3)</sub>	Horizontal Multiplexer Clock	+5.0	-5.0	V	Note 1
V $\phi$ <sub>SW</sub>	Summing Gate Clock	+5.0	-5.0	V	Note 1
V $\phi$ <sub>A(1,2,3)</sub>	Vertical Array Clocks	+3.0	-10.0	V	Note 1
V $\phi$ <sub>RG</sub>	Reset Array Clock	+5.0	-5.0	V	Note 1

Note 1:  $\phi$ S = 200pF,  $\phi$ A = 15,000pF. All clock rise and fall times should be > 10 ns.

**AC CHARACTERISTICS** Standard test conditions are nominal MPP clocks and DC operating Voltages, 1 MHz Horizontal Data Rate, 6 $\mu$ Sec Vertical shift cycle.

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V <sub>OD</sub>	Output DC Level		17.0		V	
Z	Suggested Load Register	1.0	5.0	20.0	k $\Omega$	

### PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V <sub>SAT</sub>	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity	70K	700 80K 8.0	100K	mV e- $\mu$ V/e-	Note 1
PRNU	Photo Response Non- Uniformity Peak-to-Peak		10		%V <sub>SAT</sub>	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025	<1.0	2.0	nA/cm <sup>2</sup>	Note 2
rms	Noise		5 -20		e-	

Note 1: Maximum well capacity is achieved in Buried Channel Mode.

Note 2: Values shown are for 25<sup>o</sup>C. Dark current doubles for every 5<sup>o</sup>- 7<sup>o</sup>C.

### QUANTUM EFFICIENCY ENHANCEMENTS

The STA1600 CCD area arrays can be backside thinned for increased QE. The incident illumination enters through the backside of the array, and since no photons are absorbed in the polysilicon gate structures, the QE is increased.

### COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V<sub>SAT</sub> with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The STA1600 is available in various standard grades, as well as custom selected grades. Consult Semiconductor Technology Associates for available grading information and custom selections.

### WARRANTY

Within twelve months of delivery to the end customer Semiconductor Technology Associates will repair or replace, at our option, any image sensor product if any part is found to be defective in materials or workmanship. Contact Semiconductor Technology Associates for

assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

### CERTIFICATION

Semiconductor Technology Associates certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under which it is furnished

## STA1600 Image Sensor Pad Designation

Pad#	Label	Pad#	Label	Pad#	Label	Pad#	Label	Pad#	Label
1	OS1	65	SUB	129	A1	193	S1	257	A2
2	RG	66	OS6	130	A2	194	S2	258	A1
3	SC	67	RG	131	A3	195	S3	259	SC
4	RD	68	SC	132	SUB	196	VLD	260	BB
5	SW	69	RD	133	BB	197	OTG	261	SUB
6	OTG	70	SW	134	SC	198	SW	262	A3
7	VLD	71	OTG	135	A1	199	RD	263	A2
8	S3	72	VLD	136	A2	200	SC	264	A1
9	S2	73	S3	137	A3	201	RG	265	SC
10	S1	74	S2	138	SUB	202	OS13	266	BB
11	RTN	75	S1	139	BB	203	SUB	267	SUB
12	OD	76	RTN	140	SC	204	OD	268	A3
13	SUB	77	OD	141	A1	205	RTN	269	A2
14	OS2	78	SUB	142	A2	206	S1	270	A1
15	RG	79	RG	143	A3	207	S2	271	SC
16	SC	80	SC	144	SUB	208	S3	272	BB
17	RD	81	RD	145	BB	209	VLD	273	SUB
18	SW	82	SW	146	SC	210	OTG	274	A3
19	OTG	83	OTG	147	A1	211	SW	275	A2
20	VLD	84	VLD	148	A2	212	RD	276	A1
21	S3	85	S3	149	A3	213	SC	277	SC
22	S2	86	S2	150	SUB	214	RG	278	BB
23	S1	87	S1	151	SUB	215	OS12	279	SUB
24	RTN	88	RTN	152	OD	216	SUB	280	A3
25	OD	89	OD	153	RTN	217	OD	281	A2
26	SUB	90	SUB	154	S1	218	RTN	282	A1
27	OS3	91	RG	155	S2	219	S1	283	SC
28	RG	92	SC	156	S3	220	S2	284	BB
29	SC	93	RD	157	VLD	221	S3	285	SUB
30	RD	94	SW	158	OTG	222	VLD	286	A3
31	SW	95	OTG	159	SW	223	OTG	287	A2
32	OTG	96	VLD	160	RD	224	SW	288	A1
33	VLD	97	S3	161	SC	225	RD	289	SC
34	S3	98	S2	162	RG	226	SC	290	BB
35	S2	99	S1	163	OS16	227	RG	291	SUB
36	S1	100	RTN	164	SUB	228	OS11	292	A3
37	RTN	101	OD	165	OD	229	SUB	293	A2
38	OD	102	SUB	166	RTN	230	OD	294	A1
39	SUB	103	BB	167	S1	231	RTN	295	SC
40	OS4	104	SC	168	S2	232	S1	296	BB
41	RG	105	A1	169	S3	233	S2	297	SUB
42	SC	106	A2	170	VLD	234	S3	298	A3
43	RD	107	A3	171	OTG	235	VLD	299	A2
44	SW	108	SUB	172	SW	236	OTG	300	A1
45	OTG	109	BB	173	RD	237	SW	301	SC
46	VLD	110	SC	174	SC	238	RD	302	BB
47	S3	111	A1	175	RG	239	SC		
48	S2	112	A2	176	OS15	240	RG		
49	S1	113	A3	177	SUB	241	OS10		
50	RTN	114	SUB	178	OD	242	SUB		
51	OD	115	BB	179	RTN	243	OD		
52	SUB	116	SC	180	S1	244	RTN		
53	OS5	117	A1	181	S2	245	S1		
54	RG	118	A2	182	S3	246	S2		
55	SC	119	A3	183	VLD	247	S3		
56	RD	120	SUB	184	OTG	248	VLD		
57	SW	121	BB	185	SW	249	OTG		
58	OTG	122	SC	186	RD	250	SW		
59	VLD	123	A1	187	SC	251	RD		
60	S3	124	A2	188	RG	252	SC		
61	S2	125	A3	189	OS14	253	RG		
62	S1	126	SUB	190	SUB	254	OS9		
63	RTN	127	BB	191	OD	255	SUB		
64	OD	128	SC	192	RTN	256	A3		

Pin 1

